

10/731,714

Entry is approved. 8/9/06 MZ

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 7, line ³~~2~~, with the following rewritten paragraph:

ya 9/14

- 1 For a more complete understanding of the present invention and the
2 advantages thereof, reference is now made to the following description taken in
3 conjunction with the accompanying drawings in which like reference numbers
4 indicate like features and wherein:
5 Figures 1A and 1B illustrate ~~Figure 1 illustrates~~ the scan testing circuit
6 design for a SoC in accordance with the present invention;
7 Figures 2 displays the clock control mechanism implemented in the scan
8 testing circuit design of Figure 1;
9 Figures 3 shows the scan enable registering logic of Figure 1;
10 Figure 4 illustrates the clock generator for scan chain group A of Figure 1;
11 Figure 5 shows the clock generator for scan chain group B of Figure 1;
12 Figure 6 displays the clock generator for scan chain group C of Figure 1;
13 Figure 7 illustrates the test mode select arrangement for the test mode
14 delta signal TM_{Δ} of Figure 2;
15 Figure 8 illustrates the test mode select arrangement for the simultaneous
16 test mode signal TM_{ALL} and intermediate control signals, sig_A, sig_B, and sig_C
17 ~~of Figure 2~~; and
18 Figure 9 displays the test mode select arrangement for the first, second
19 and third test mode signals, TM_1 , TM_2 , and TM_3 , and the VLCT mode signal
20 $VLCT_M$ of Figure 2.

Please replace the paragraph beginning at page 8, line 23, with the following rewritten paragraph:

- 1 Figure 1A + illustrates the scan test circuit design for a mixed signal SoC
2 in accordance with the present invention. For simplicity, Figure 1A + clearly